ABSTRACT OF THE DISCLOSURE

By an NMOS (22) being switched on or off, a direct-current voltage E_0 is charged in a capacitor (24), and a DC/DC converting circuit (30) charges a direct-current output voltage V_0 to be supplied to a load L in a capacitor (34). A load state detection circuit (40) determines whether the load L is in a lightly loaded state or in a non-lightly loaded state, and outputs a signal (S40) as a determination signal. When the load state detection circuit (40) outputs a signal (S41) of "L" as a signal representing that it is a lightly loaded state, a time period setting circuit (41) outputs a signal (S41) of "L" after a preset time period elapses. A PFC on/off switching circuit (42) is supplied with the signal (S41) of "L", and outputs a control signal (S25) of "L" to a power factor improvement circuit (20). Accordingly, in the case where the load L enters a lightly loaded state, the operation of the power factor improvement circuit (20) is stopped when the preset time elapses.